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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,683	09/23/2003	Andre Schaefer	30169/30001	1058

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EXAMINER	
TON, MY TRANG	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,683	SCHAEFER ET AL.	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 10-12 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim Rejections - 35 USC § 112

Claims 2 and 8-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, there is no support for the language "further connection" recited in line 1 and "further clock pulse" recited in line 2 since there is no other "connection" or "clock pulse" recited.

Claim 8 recites the limitation "the comparison device" in line 3. There is insufficient antecedent basis for this limitation in the claim.

In claim 9, it is unclear as to whether "a clock pulse" recited in line 4 is additional limitation "a clock pulse" as previously cited in claim 2, lines 2-3.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Kawasaki et al (U. S Patent No. 6,433,607) (Ref. No. 2001/0043099 cited in PTOL 1449).

Kawasaki et al disclose in Figs. 17 and 19 an input circuit including:

a circuit device (21) with at least one connection (connection connected to 220), to which a clock pulse (CLK) can be applied, characterized in that the circuit device (21) also comprises a clock pulse detection facility (220) to determine whether there is a clock pulse (CLK) present at the connection (when CLK present, pulse will be provided) as recited in claim 1.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1- 2 and 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Jong et al (U. S Patent No. 6,737,892).

Jong et al disclose in Fig. 3 a system for detecting a valid clock signal at a clock receiver including:

Regarding claim 1: a circuit device (101, Fig. 1) with at least one connection (CK+122 or CK+123), to which a clock pulse (CK+122 or CK+123), characterized in that the circuit device (101) also comprises a clock pulse detection facility (120) to determine whether there is a clock pulse (CK+122 or CK+123) present at the connection (detecting a valid clock signal: see col. 4, lines 16-21, lines 58-63, col. 5, lines 12-48).

Claim 2 is similarly rejected as claim 1:

A circuit device (101, Fig. 1) with at least one further connection (CK-123), to which a further clock pulse (CK-123) can be applied, whereby in determining whether a clock pulse (CK+122) is present at the connection, it is determined whether there are differential clock pulses (CK+122, CK-123) present at the connections, or whether there is a single clock pulse present at the further connection, but not at the connection (detecting a valid click signal: see col. 4, lines 16-21, lines 58-63, col. 5, lines 12-48).

The semiconductor component (101) that comprises at least one circuit device (120) as recited in claim 10.

The limitation recited in claims 11-12 are seen to define intended use. The clock detection circuit of Jong is capable of using for DDR memory component and the memory component is a DRAM as recited. **In re Tuominen, 213 USPQ 89 (CCPA 1982) & In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974).**

Claims 1- 7, 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Hattori (U. S Patent No. 6,791,369).

Hattori disclose in Figs. 6-8 a differential-clock detector circuit including:

Regarding claim 1: a circuit device (40) with at least one connection (CK+ or CK-) to which a clock pulse (CK+ or CK-), characterized in that the circuit device (40) also comprises a clock pulse detection facility (40) to determine whether there is a clock pulse (CK+ or CK-) present at the connection (presence or absence of the differential clock is detected, see col. 5, line 15 – col. 6, line 39).

Claim 2 is similarly rejected as claim 1:

A circuit device (40) with at least one further connection (CK-), to which a further clock pulse (CK-) can be applied, whereby in determining whether a clock pulse (CK+) is present at the connection, it is determined whether there are differential clock pulses (CK+, CK-) present at the connections, or whether there is a single clock pulse present at the further connection, but not at the connection (presence or absence of the differential clock is detected, see col. 5, line 15 – col. 6, line 39).

Regarding claim 3:

a comparison device (82-84, Fig. 6) for comparing the signal present at the connection (CK+) in particular the clock pulse (CK+) applied thereto, with a reference signal (VCM).

The comparison device (82, 84) comprises a differential amplifier as recited in claim 4.

Regarding claim 5: the comparison device (82, 84) emits a pulse, more specifically a clock pulse detection signal, when the level of the signal present at the connection (CK+) exceeds or falls below a predetermined level (Fig. 6 capable of providing exceeds or fall below a predetermined level VCM), in particular, the level of the reference signal (VCM).

Claims 6-7 are similarly rejected as claim 5: Fig. 6 is capable of providing such function recited therein.

The semiconductor component (Fig. 7-8) that comprises at least one circuit device (Fig. 6) as recited in claim 10.

The limitation recited in claims 11-12 are seen to define intended use. The clock presence detector circuit of Hattori is capable of using for DDR memory component and memory component is a DRAM as recited. **In re Tuominen, 213 USPQ 89 (CCPA 1982) & In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974).**

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-12 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of copending Application No. 10/658,741. Although the conflicting claims are not identical, they are not patentably distinct from each other because the copending Application claims a component including a connection, at least one further connection, differential input clock pulses or a single input clock pulse can be applied to the connection and/or the further connection, a circuit device to detect whether differential input clock pulses are present at the connections, a comparison device comparing signal present at the connection with a reference signal, a counter device, DDR semi-conductor memory

component, memory component is a DRAM wherein the instant application is now also claiming an apparatus which includes all of the elements of the copending application claims (for example: at least one connection, at least one further connection, differential input clock pulses or a single input clock pulse can be applied to the connection and/or the further connection, a circuit device to detect whether differential input clock pulses are present at the connections, a comparison device comparing signal present at the connection with a reference signal, a counter device, DDR semi-conductor memory component, memory component is a DRAM).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MY-TRANG NU TON
PRIMARY EXAMINER

December 7, 2004